

FIG.1

200

SETUP AND HOLD	
WARNING: WHEN THE SETUP AND HOLD SPECIFICATION FOR A LABEL IS CHANGED, THIS IMPACTS ALL OTHER LABELS THAT INCLUDE THE SAME CHANNELS.	
ADDR DATA	<input type="checkbox"/> ALL BITS ~ 220 <input type="checkbox"/> INDIVIDUAL BITS
	BIT: <input type="text" value="0"/> <input type="button" value="▲"/> SETUP: <input type="text" value="1 2.500 ns"/> <input type="button" value="▲"/> HOLD: <input type="text" value="1 0 s"/> <input type="button" value="▲"/>
<input type="button" value="OK"/> 210 <input type="button" value="CANCEL"/>	

FIG.2

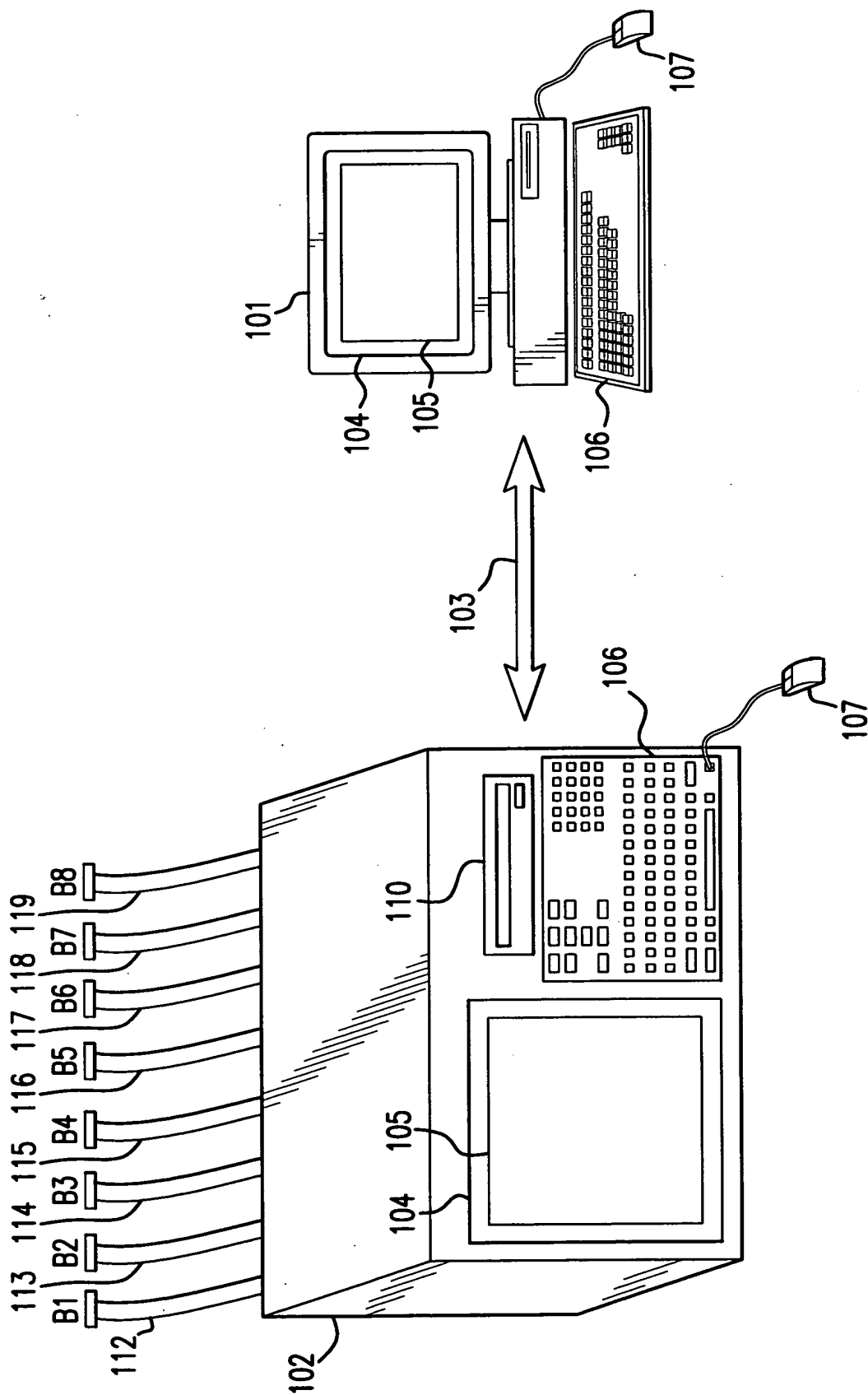
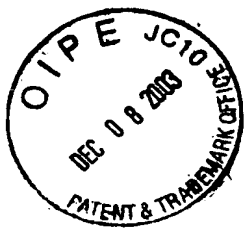


FIG. 3

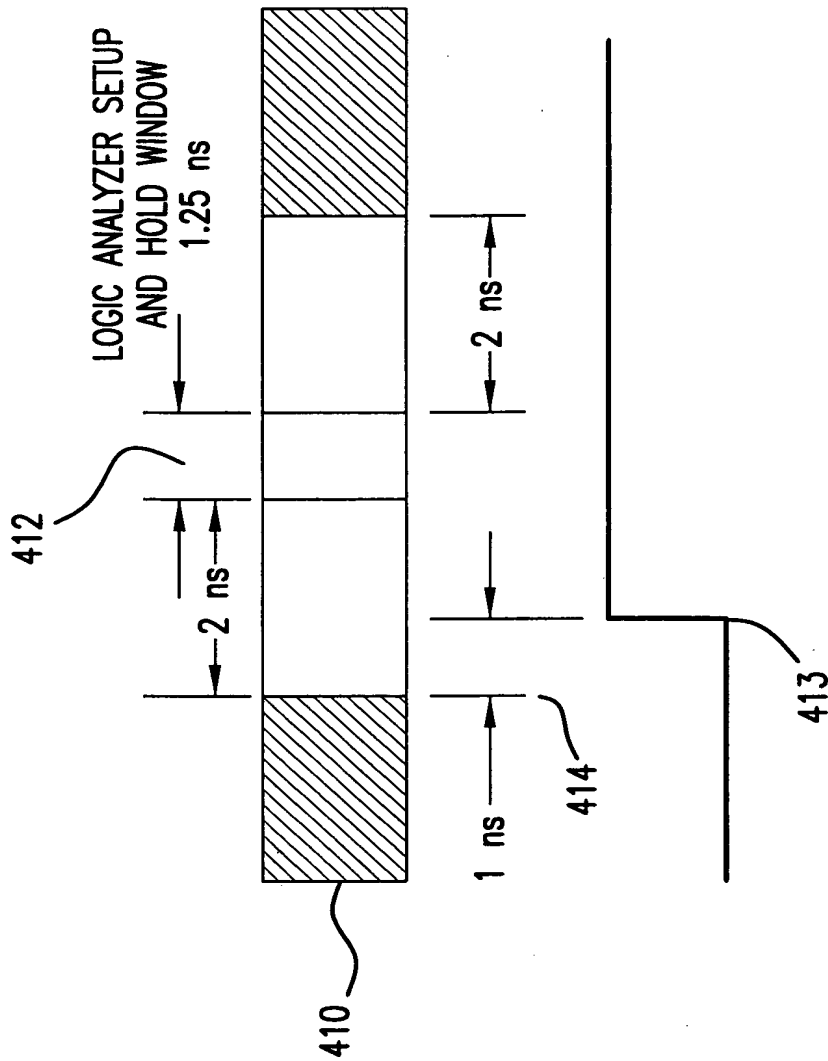
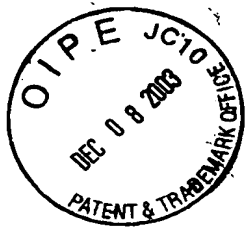


FIG.4

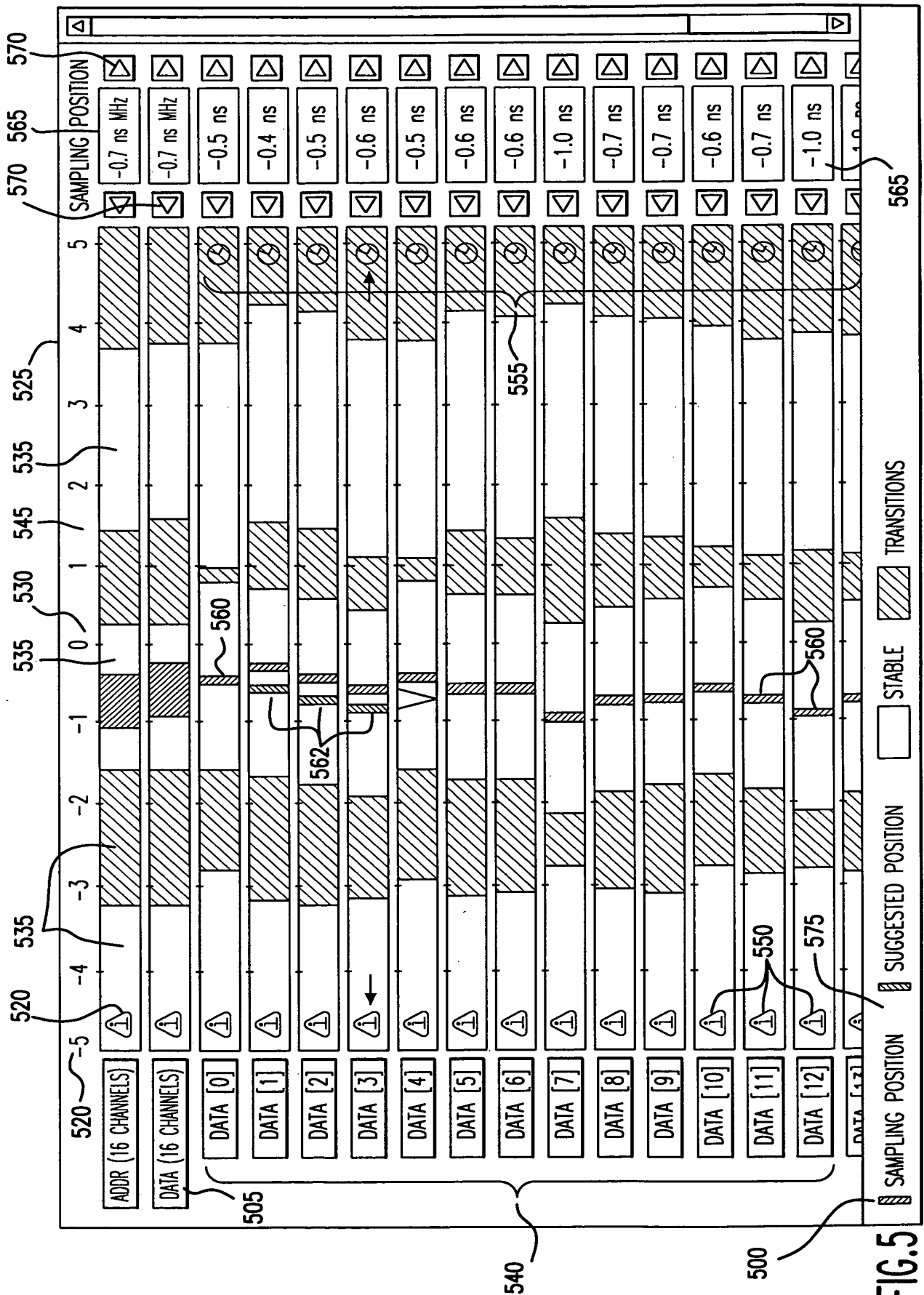
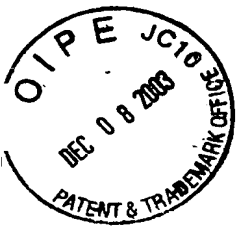


FIG. 5

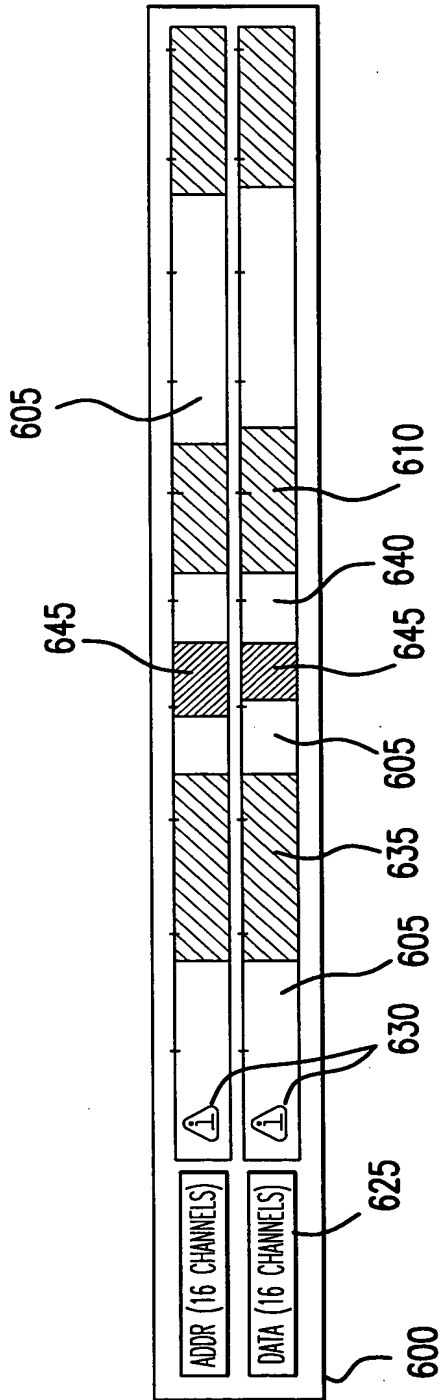
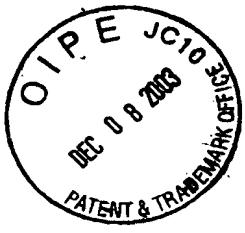


FIG. 6

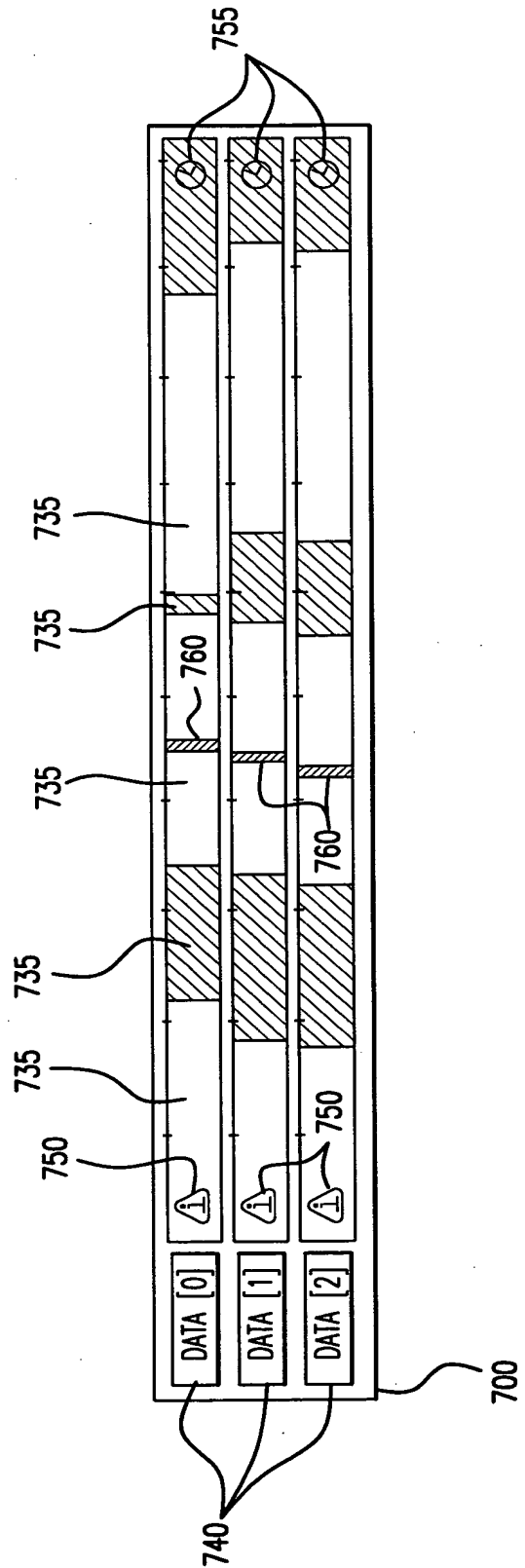


FIG. 7

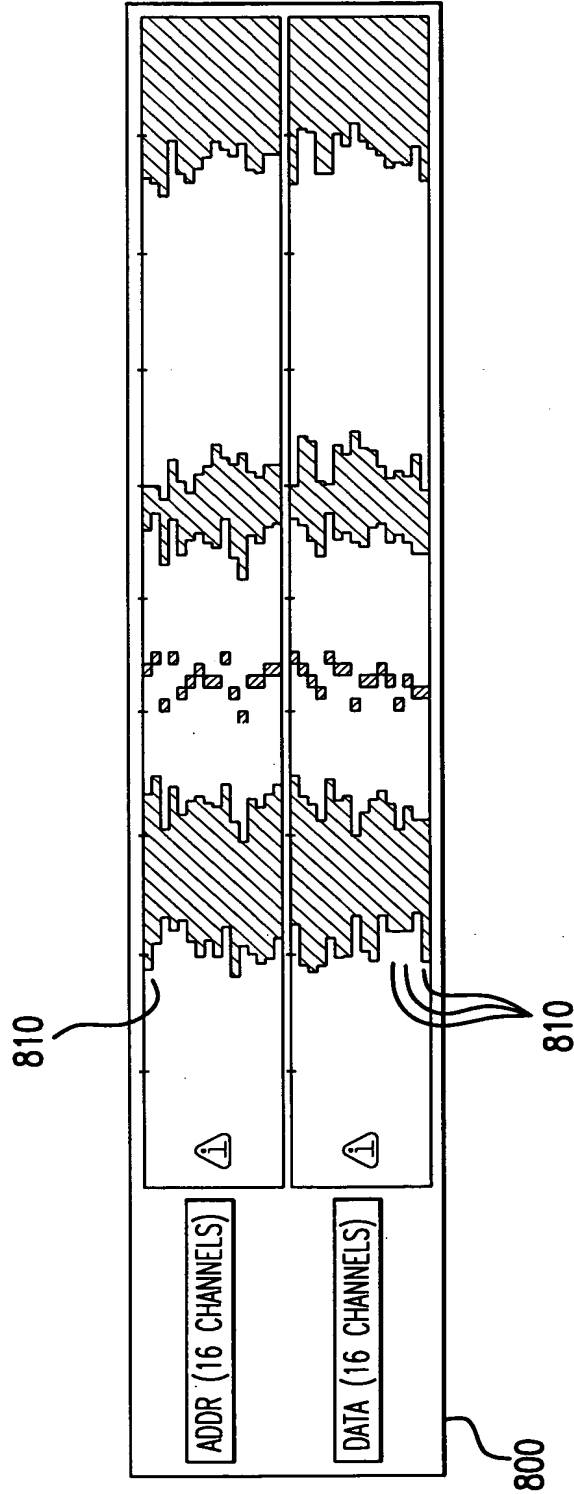
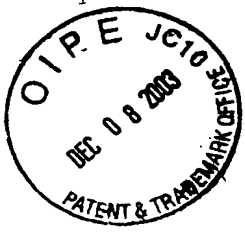
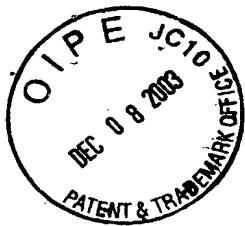


FIG. 8



Agilent Technologies, Inc

Docket No. 10001979-1

Title: Signal Transition And Stable Regions Diagram For  
Positioning A Logic Analyzer Sample

Inv. David N. Sontag, et al

8 pp (figs. 1-12)

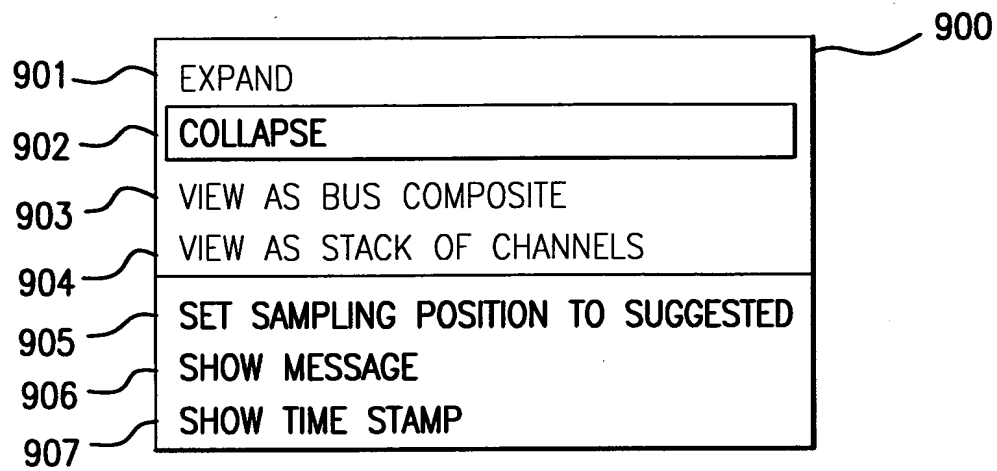


FIG.9

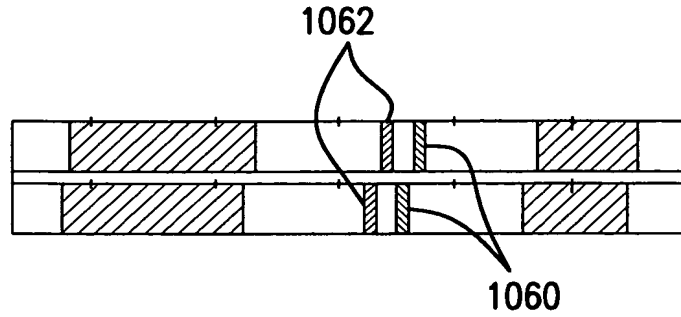
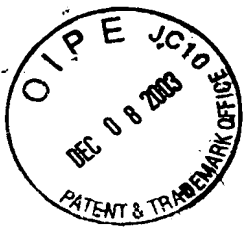


FIG. 10

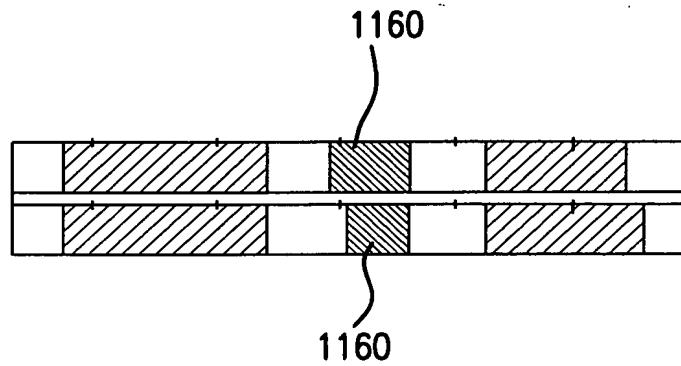


FIG. 11

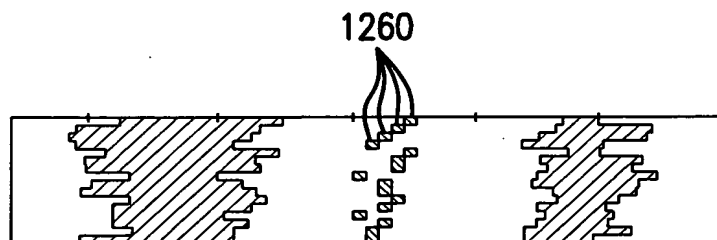


FIG. 12